SEMESTER I

15LV01 GRAPH THEORY AND OPTIMIZATION TECHNIQUES

2 2 0 3

BASIC CONCEPTS IN GRAPH THEORY: Undirected graph – degree of a vertex, degree sequence, sub graphs, vertex induced subgraphs, complement of a graph, self complementary graphs, walk, path, connectivity, eccentricity, radius, diameter, vertex and edge cuts, vertex partition, independent set, clique. Digraph – orientation, strongly, weekly and unilaterally connected digraphs, directed acyclic graph. Adjacency matrix and incidence matrix of graphs. Trees, Spanning trees, Matrix tree theorem. (7 + 7)

GRAPH ALGORITHMS: Search algorithms – depth first search and breadth first search, spanning tree algorithm – Kruskal's and Prim's shortest path algorithm – Dijkstra's and Floyd-Warshall. Matching – perfect matching, bipartite matching. Flow networks – augmenting path algorithm, min-cut and max-cut algorithms. (7 +7)

LINEAR PROGRAMMING: Formulation, simplex method, two phase method, simplex multipliers, dual and primal, dual simplex method. (4+4)

DYNAMIC PROGRAMMING: Principle of optimality, backward and forward induction methods, calculus method of solution, tabular method of solution, shortest path network problems, applications in production. (6+6)

NONTRADITIONAL OPTIMIZATION ALGORITHMS: Genetic Algorithm – Working Principle – Comparison between GA and traditional method – GA operators - GA for constrained optimization. Ant colony optimization: Ant's foraging behaviour and optimization, artificial ants and minimum cost paths, traveling salesman problem, ACO algorithm for traveling salesman problem. (6+6)

Total L: 30 + T: 30 = 60

REFERENCES:

1. Jonathan L Gross and Jay Yellen, "Graph Theory and its Applications", Chapman & Hall, New York, 2005.
2. West D B, "Introduction to graph Theory", Pearson Education, New Delhi, 2007.
3. Hamdy A Taha, "Operations Research: An Introduction", Pearson Education, New Delhi, 2014.
4. Kalyanmoy Deb, "Optimization for Engineering Design, Algorithms and Examples", Prentice Hall, New Delhi, 2010.
5. Marco Dorigo and Thomas Stutzle, "Ant Colony Optimization", Prentice Hall, New Delhi, 2005.

15LV02 DIGITAL DESIGN PRINCIPLES

3 0 0 3

COMBINATIONAL CIRCUITS: Design using Multiplexers - Decoders - Design using PLDs. (8)

SEQUENTIAL CIRCUITS: Synchronous circuits - Mealy machine, Moore machine, State diagrams, State table minimization, State assignments, Clocked Circuits using Flip Flops. The ASM chart - Design from an ASM chart: Boolean implementation for minimal number of Flip-Flops - Design from an ASM chart: One-Hot controller implementation: state table entry to a PLD - clock skew in state machines - Initialization and lockout in state machines. (9)

Asynchronous Circuits: Analysis - Circuits with latches - Design - Reduction of State and Flow Tables - Race Free State Assignment – Hazards. (10)

DATAPATH AND CONTROL PATH DESIGN: Data paths and operations - Micro operations - multiplexer based transfer-arithmetic/logic unit – the shifter - Data path representation - pipelined data path - The control unit - Design example: Binary Multiplier - Hardwired control - Micro programmed control. (10)

VHDL: Entities and architectures - Behavior, dataflow and structural modeling, writing Test benches. (8)

Total L: 45

REFERENCES:

1. Morris Mano, "Logic and computer design fundamentals", Pearson education, 2008.
2. James E Palmer and David E Perlman, "Introduction to Digital Systems", Tata McGraw Hill, 2004.
3. Bhasker J, "A VHDL Primer", Prentice Hall, 1999.
4. Charles H Roth, "Digital system Design with VHDL", Thomson, 2003.

15LV03 DEVICE MODELING

3 0 0 3

INTRODUCTION TO SEMICONDUCTOR PHYSICS AND PASSIVE DEVICES: Review of Quantum Mechanics - Boltzman transport equation - Continuity equation - Poisson equation - Types and Structures of resistors and capacitors in monolithic technology - dependence of model parameters on structure. (9)

INTEGRATED DIODES: Junction and Schottky diodes in monolithic technologies - static and dynamic behavior - small and large signal models - SPICE models. (8)

INTEGRATED BIPOLAR TRANSISTOR: Types and structures in monolithic technologies - Basic model (Eber - Moll) - Gunmel - poon model - dynamic model, parasitic effects - SPICE model - parameter extraction. (9)

INTEGRATED MOS TRANSISTOR: nMOS and PMOS Transistor - Threshold voltage - Threshold voltage equations - MOS device equations - Basic DC equations Second order effects - MOS models - Small signal AC Characteristics - MOSFET SPICE model, EKV Model, BSIM Model, Modeling for RF applications. (10)

VLSI FABRICATION TECHNIQUES: An overview of wafer fabrication, wafer processing- oxidation - patterning - Diffusion - Ion implantation - Deposition - Silicon Gate nmos process - CMOS process - nwell - pwell -Twin tub - Silicon on Insulator - CMOS process enhancements - Interconnects circuit elements. EMI environment: Sources of EMI and EMC, Definitions and units of parameters, Radiation hazards to human beings. (9)

Total L: 45

REFERENCES

1. Sze S M and Kwok K Ng, “Physics of Semiconductor Devices”, John Wiley and Sons, 2006.
2. Ben G Streetman, "Solid State Circuits", Prentice Hall, 1997.
3. Tyagi M S, "Introduction to Semi-conductor Materials and Devices", John Wiley, 2008.
4. Tor A Fijedly, “Introduction to Device Modeling and Circuit Simulation”, Wiley-Interscience, 2007.
5. Daniel Foty, “MOSFET Modeling with SPICE", Prentice Hall, 2007.

15LV04 DIGITAL IC DESIGN

3 0 0 3

OVERVIEW OF VLSI DESIGN METHODOLOGY: VLSI design process - Architectural design - Logical design-Physical design-Layout styles - Full custom, Semicustom approaches. layout design rules**:** Need for design rules – Layer representations - CMOS nwell / pwell design rules – Design rule backgrounder-Layer assignments - SOI rules. (9)

MOS INVERTER: Static characteristics - Resistive load inverter - Inverter with n-type MOSFET load - CMOS inverter - Transient characteristics - Delay time definitions, calculation of delay times. (8)

LOGIC DESIGN: Static CMOS Design - Complementary CMOS, Ratioed logic, Pass transistor and transmission gate - Dynamic CMOS logic - . CMOS logic - Precharged domino logic. (9)

SEQUENTIAL LOGIC: Static Sequential circuits - Bistatbility, CMOS static FF, Dynamic sequential circuits – Pseudo static latch, Dynamic two phase FF, Clocked- CMOS latch, NORA CMOS logic, TSPCL logic. (9)

VLSI BUILDING BLOCKS DESIGN: Adders, Shifters, Arithmetic logic unit design, Multipliers-Array, Carry Save multiplier, Wallace tree, Booth's algorithm, Modified Booths Algorithm. Designing Memory and Array Structures-Memory peripheral circuit. (10)

Total L: 45

REFERENCES:

1. Jan M Rabaey, “Digital Integrated Circuits", Prentice Hall, 2004.
2. Kang, “CMOS Digital integrated Circuits”, McGraw Hill, 2003.
3. Saida M Sait and Habib Youssef, “VLSI Physical Design Automation: Theory and Practice”, World Scientific Publishing Company, 1999.
4. Douglas A Pucknell, Kamran Eshraghian, "Basic VLSI Design", PHI learning, New Delhi, 2011.
5. Neil Weste and David Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, Pearson, 2010.

15LV05 DESIGNING WITH FPGAS

3 2 0 4

VERILOG: Signals, Identifier , Net and variable types, Operators, Gate instantiations, Modules and ports, data flow, gate level, Behavioral level ,Switch level and state machine modeling , Concurrent and procedural statements, UDP, sub circuit parameters, function and task, timing and delays - test benches-design of combinational and sequential circuits using Verilog. (10+10)

CLOCKING AND METASTABILITY: Set up time hold time – setup time hold time violations-critical path -calculation of maximum clock frequency –metastability-synchronizers-design examples. (8)

FPGA ARCHITECTURES: Design flow using FPGAs, Role and Types of CAD Tools - Architecture of Xilinx and Altera FPGAs – configurable logic blocks, I/O blocks - programmable interconnections - clock circuits – programming technologies – antifuse, SRAM, EPROM, EEPROM - Implementation using FPGA – timing models - calculation of path delay - power analysis. (8)

DATA PATH AND MEMORY DESIGN: Design of memories - ROM, single and dual port RAM - synchronous and asynchronous read - arithmetic circuit design - serial/parallel adder, subtractor, floating point adder/subtractor multiplier - sequential multiplier, array multiplier, signed multiplier - ALU. (9+10)

CONTROLLER AND DSP DESIGN: Memory controller, processor control unit, communication controllers - UART, I^2C, VGA controller, USB, DSP blocks- FIR and IIR filters. (10+10)

Total L: 45 + T: 30 = 75

TUTORIAL COMPONENT:

1. Modeling and simulation of combinational and sequential circuits using Verilog.
2. Design and Implementation of arithmetic circuits.
3. Design and implementation of real time clock and controller.
4. Design and implementation of memory modules and filters.
5. Interfacing with ADC/DAC and display modules.

REFERENCES:

1. Bhasker J, "A Verilog Primer", Prentice Hall, 2005.
2. Michael D Ciletti, "Advanced Digital Design with Verilog HDL", Pearson education, 2005.
3. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Prentice Hall, 2003.
4. Seetharaman Ramachandran, "Digital VLSI systems design", Springer, 2011.
5. Charles H Roth, "Digital System Design using VHDL", Thomson, 1998.

15LV51 VLSI DESIGN LABORATORY

0 0 2 1

In this course the students will be provided with an orientation program on the following equipment/software for duration of 4 hours. After this orientation each student is expected to formulate a complete an activity of interest which has to be derived from the orientation program under the guidance of a faculty. The details like background, problem definition, state of technology/ knowledge in that area by a good literature review (5 latest papers), objectives, methodology, equipment that can be used from the orientation program, results from the experiments and their interpretation with respect to the assumptions or background and a formal conclusion are expected in the report which is to be submitted at the end of the semester. This work is evaluated for the credit assigned. Expected hours needed for this work is 26 hours.

- Study of MOS and Inverter characteristics
- Design of static and dynamic digital circuits
- Design of combinational circuits
- Design of sequential circuits
- Design of Memories with Peripherals
- Model parameter extraction for diode, BJT, MOSFET
- Layout generation from schematics

Total P: 30

15LV61 INDUSTRY VISIT & TECHNICAL SEMINAR

0 0 4 2

The student will make at least two technical presentations on current topics related to the specialization. The same will be assessed by a committee appointed by the department. The students are expected to submit a report at the end of the semester covering the various aspects of his/her presentation together with the observation in industry visits. A quiz covering the above will be held at the end of the semester.

Total P: 60

SEMESTER II

15LV06 LOW POWER VLSI DESIGN

3 0 0 3

INTRODUCTION: Need for Low power VLSI chips - Low Power Design Methodology - Logic synthesis for Low power - Sources of Power dissipation. (9)

POWER ANALYSIS AND ESTIMATION: Gate level Analysis, Architecture level Analysis, Data Correlation Analysis, Monte-Carlo Simulation, Probabilistic Power Analysis. Statistical Techniques - Estimation of Glitching Power - Sensitivity Analysis - Circuit

Reliability - Power Estimation at the circuit level - High level Power Estimation - Information Theory based approaches - Estimation of maximum power. (10)

POWER OPTIMISATION TECHNIQUES: Circuit Level – Transistor and Gate Sizing, Equivalent Pin Ordering, Network Restructuring and Reorganization, Special Latches and Flip Flops, Low Power Digital Cell Library, Adjustable Device Threshold Voltage. Leakage current in deep sub micrometer transistors- Transistor Leakage Mechanism, Leakage Current Estimation. Logic Level – Gate Reorganization, Signal Gating, Logic Encoding, State Machine Encoding, Precomputational Logic. Architectural and System Level – Power and Performance Management, Switching Activity Reduction, Parallel Architecture with Voltage Reduction, Flow Graph Transformation. Advanced Techniques- Adiabatic Computation, Pass Transistor Logic Synthesis, Asynchronous Circuits, Low power bus – low swing bus, charge recycling bus, delay balancing. (10)

LOW POWER STATIC RAM ARCHITECTURES: Organization, MOS Static RAM Memory Cell, Banked Organization, Voltage Swing Reduction, Power Reduction. (9)

LOW VOLTAGE CMOS VLSI TECHNOLOGY: BICMOS and Silicon On Insulator (SOI) Technology. (7)

Total L: 45

REFERENCES:

1. Kaushik Roy and Sharat C Prasad , “Low Power CMOS VLSI circuit Design”, John Wiley and Sons, 2000.
2. Gary B Yeap K, "Practical Low Power Digital VLSI Design”, Kluwer Academic Publishers, 1998.
3. Kuo J B and Lou J H, “Low Voltage CMOS VLSI Circuits”, John Wiley and Sons, Singapore, 1999.
4. Anantha P Chandrakasan and Robert W Brodersen, “Low Power Digital CMOS Design”, Kluwer Academic Publishers, Holland, 1995.

15LV07 ANALOG VLSI CIRCUITS

3 2 0 4

ANALOG CIRCUIT BUILDING BLOCKS: Current mirrors/amplifiers - Voltage and current references, Comparator, Multiplier. (9+6)

AMPLIFIERS:MOS and BJT inverting amplifier - Improving performance of inverting amplifier - CMOS and BJT differential amplifiers - Characterization of Op-Amp - The BJT two stage op-amp - The CMOS two stage op-amp -Op-amps with output stage, Folded Cascode op-amp, Transconductance Amplifier-Noise and Distortion in Amplifiers. Phase Locked Loops – Phase Detector-VCO-Loop Filter. (10+8)

DATA CONVERTER FUNDAMENTALS: Ideal A/D and D/A converters, Quantization noise, Signed codes, Performance limitations. (9+6)

D/A AND A/D CONVERTERS: D/A converter : Current scaling, Voltage scaling and Charge scaling D/A converters -Serial D/A converters -Serial A/D converters, Parallel - High performance A/D converters. (9+6)

LAYOUT ISSUES: CMOS design rules - layout of CMOS - BJT- Capacitors – Resistors - Mixed layout issues: Floor planning, power supply & ground, fully differential matching, Guard rings and shielding. (8+4)

Total L: 45 + T: 30 = 75

TUTORIAL COMPONENT:

1. Design and Simulation of analog basic building blocks.
2. Design and Simulation of Amplifiers.
3. Design and Simulation of data converters.
4. Design and Simulation of PLL.

REFERENCES:

1. Randall L Geiger, Phillip E Allen and Noel R Strader, "VLSI Design Techniques for Analog and Digital Circuits", McGraw Hill, International Edition, 2010.
2. David A Johns and Ken Martin, “Analog Integrated Circuit Design”, John Wiley and Sons, 2008.
3. Phillip Allen and Douglas Holberg, “CMOS Analog Circuit Design”, Oxford University Press, 2012.
4. Benhard Razavi, “Data Converters”, Kluwer Publishers, 2005.
5. Paul R Gray and Robert G Meyer “Analysis and Design of Analog Integrated Circuits”, John Wiley and Son, 2005.

15LV08 TESTING AND TESTABILITY

3 0 0 3

INTRODUCTION: Motivation for testing and design for testability - Fault models -Fault simulation techniques-Serial, Single-fault propagation, Deductive, Parallel and Concurrent Simulation. (8)

COMBINATIONAL CIRCUIT TESTING: Test generation algorithms for combinational logic circuits - Fault Table, Boolean difference, Path sensitization, D - algorithm PODEM, FAN algorithms. (8)

SEQUENTIAL CIRCUIT TESTING: Functional testing –Fault model based testing- Time frame expansion, Key testability concepts – Ad Hoc design for Testability – scan based design - Signature analysis - Compression techniques-Built-in self-test -Architectures-Boundary scan standard. (10)

ANALOG AND MIXED SIGNAL TEST: Analog testing difficulties, Fault models, Analog fault simulation, ADC and DAC testing methods-Analog test bus standard. (10)

SPECIAL TESTING PROBLEMS: System test - functional test - diagnostic test - core based design and test wrapper - test architecture for SOC - Testability features for board test - FPGA testing. (9)

Total L: 45

REFERENCES:

1. Vishwani D Agarwal, "Essential of Electronic Testing for Digital, Memory and Mixed Signal Circuits", Springer, 2002.
2. Wang, Wu and Wen, "VLSI Test Principles and Architectures", Morgan Kaufmann, 2006.
3. Abramovici M, Breuer M A and Friedman A D, "Digital Systems Testing and Testable Design", Wiley, 1994.
4. Robert J Feugate and Jr Steven M, "Introduction to VLSI Testing", Prentice Hall, Englewood Cliffs, 1998.
5. Parag K Lala, "Digital Circuit Testing and Testability", Academic Press, 1997.

15LV09 COMPUTER AIDED DESIGN OF VLSI SYSTEMS

3 0 0 3

INTRODUCTION: VLSI Design cycle - Role of CAD tools in the VLSI Design process -data structures and algorithms: Complexity of algorithms, dynamic programming, Integer linear programming, Genetic algorithm, Simulated Annealing. (9)

SIMULATION & SYNTHESIS: Compiler driven simulation-Event driven simulation - Switch level simulation - Circuit simulation - logic synthesis – two level synthesis, Binary decision diagrams, and ROBDD principles. (9)

PHYSICAL DESIGN AUTOMATION: Partitioning - KL, FM algorithms, Placement – Simulation based algorithms- Simulated Annealing , Force Directed Algorithm, Partitioning based algorithms- Breuer's Algorithm, Terminal propagation Algorithm , Cluster Growth Algorithm , Floor planning – slicing floor plan , Constraint Based Floor Planning, Integer Program Based Floor Planning – Pin Assignment. (9)

ROUTING: Grid routing – Maze Routing Algorithms, Global routing - Shortest Path Based Algorithms, Steiner tree based Algorithms, detailed routing – Left Edge algorithm, Dog-Leg Algorithm , Greedy Channel Routing, Switch Box Routing algorithms-over the cell routing, Clock Routing. (9)

LAYOUT SYNTHESIS AND OPTIMISATION: Layout generation and Optimization of standard cell layout, gate matrix layout and PLA, Layout Compaction – one dimensional and two dimensional compaction. (9)

Total L: 45

REFERENCES:

1. Sherwani Sherwani N A, "Algorithms for VLSI Physical Design Automation", Kluwer, 2007.
2. Sait S M and Youssef H, "VLSI Physical Design Automation", World Scientific, 2004.
3. Sabih H Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2008.
4. Micheli G D, "Synthesis and Optimization of Digital Circuits", Tata McGraw Hill, 2003.

15LV10/15LC25 VLSI SIGNAL PROCESSING

3 2 0 4

REALIZATION OF DIGITAL FILTERS: FIR filter design - IIR filter design - Direct form I, II, Cascade, parallel, Ladder - Lattice filters. (11)

ITERATION BOUND: Introduction, Data flow graph representations, loop bound and iteration bound, Algorithms for computing Iteration bound, iteration Bound of multirate Data - Flow Graphs. (8+6)

PIPELINING AND PARALLEL PROCESSING: Introduction - Pipelining of FIR Digital filters - Parallel processing - Pipelining and parallel processing for Low power. (9+6)

TRANSFORMATIONS-RETIMING**:** Introduction - Definitions and Properties - Solving system of Inequalities - Retiming Techniques. UNFOLDING: Introduction - An algorithm for unfolding - Properties of unfolding - Critical path, unfolding and retiming - Application of unfolding. FOLDING: Introduction - folding Transformation - Register Minimization Techniques - Register Minimization in folded Architectures. (10+11)

FAST CONVOLUTION: Cook - Toom algorithm –modified Cook - Toom algorithm Winogard algorithm- modified Winogard algorithm, Algorithmic strength reduction in filters and transforms-parallel FIR filters, Parallel architectures for Rank-order filter. (8+6)

Total L: 45 + T: 30 = 75

TUTORIAL COMPONENT:

1. Design of Digital filters.
2. Pipelining/Parallel processing of filter.
3. Design and implementation of Lattice filter using Retiming techniques.
4. Design and implementation of filter using Unfolding techniques.
5. Design and implementation of Low power IIR/Lattice filter.

REFERENCES:

1. Keshab K Parhi, "VLSI Digital Signal Processing Systems Design and Implementation", Wiley - Inter science, 2007.
2. John G Proakis and Dimitris G Manolakis, "Digital signal processing – Principles, Algorithms and Applications" Pearson, 2011.
3. Lonnie C Ludeman, "Fundamentals of Digital Signal Processing", Wiley India (P) Ltd., 2010.
4. Uwe Meyer Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer, 2014.
5. Peter Pirsch "Architectures for Digital Signal Processing", Wiley India (P) Ltd., 2009.

15LV52 ADVANCED VLSI DESIGN LABORATORY

0 0 2 1

In this course the students will be provided with an orientation program on the following equipment/software for duration of 4 hours. After this orientation each student is expected to formulate a complete an activity of interest which has to be derived from the orientation program under the guidance of a faculty. The details like background, problem definition, state of technology/ knowledge in that area by a good literature review (5 latest papers), objectives, methodology, equipment that can be used from the orientation program, results from the experiments and their interpretation with respect to the assumptions or background and a formal conclusion are expected in the report which is to be submitted at the end of the semester. This work is evaluated for the credit assigned. Expected hours needed for this work is 26 hours.

- Specification, Design, synthesis and layout design (floorplanning, place and route, power and clock distribution, clock tree synthesis, timing analysis, power analysis, signal integrity, post-layout simulation and back annotation, GDS-II generation) of digital building block.
- Specification, Schematic Design, simulation, layout generation, Physical verification (LVS, DRC, RC extraction, post layout simulation, back annotation, GDS-II generation) of analog building block.

Total P: 30

SEMESTER III

15LV53 HIGH LEVEL VERIFICATION AND TESTING LABORATORY

0 0 2 1

In this course the students will be provided with an orientation program on the following equipment/software for duration of 4 hours. After this orientation each student is expected to formulate a complete an activity of interest which has to be derived from the orientation program under the guidance of a faculty. The details like background, problem definition, state of technology/ knowledge in that area by a good literature review (5 latest papers), objectives, methodology, equipment that can be used from the orientation program, results from the experiments and their interpretation with respect to the assumptions or background and a formal conclusion are expected in the report which is to be submitted at the end of the semester. This work is evaluated for the credit assigned. Expected hours needed for this work is 30 hours.

- Introduction to UNIX commands and Writing Shell scripts.
- High Level Modeling using SystemVerilog.
- High Level Verification using SystemVerilog.
- Test Pattern Generation using ATPG.
- Modeling DFT and BIST architectures.

Total P: 30

15LV71 PROJECT WORK - I

0 0 6 3

- ❖ Identification of a real life problem in thrust area
- ❖ Developing a mathematical model for solving the above problem
- ❖ Finalization of system requirements and specification

- Proposing different solutions for the problem based on literature survey
- Future trends in providing alternate solutions
- Consolidated report preparation of the above

Total P: 90

SEMESTER IV

15LV72 PROJECT WORK – II

0 0 28 14

- The project work involves the following:

Preparing a project- brief proposal including
- Problem identification
- A statement of system / process specifications proposed to be developed (Block Diagram/ Concept tree)
- List of possible solutions including alternatives and constraints
- Cost benefit analysis
- Time line of activities

- A report highlighting the design finalization [based on functional requirements & standards (if any)]

A presentation include the following
- Implementation phase(Hardware / Software / both)
- Testing and validation of the developed system
- Learning in the Project

- Consolidated report preparation.

Total P: 420

ELECTIVE THEORY COURSES

15LV21 MIXED SIGNAL VLSI DESIGN

3 0 0 3

INTRODUCTION TO ACTIVE FILTERS & SWITCHED CAPACITOR FILTERS: Switched capacitor filters: Switched capacitor resistors - amplifiers – comparators - sample & hold circuits – Integrator- Biquad. (9)

CONTINUOUS TIME FILTERS: Introduction to Gm - C filters - bipolar transconductors - CMOS Transconductors using Triode transistors, active transistors - BiCMOS transconductors – MOSFET C Filters - Tuning Circuitry - Dynamic range performance - Elementary transconductor building block- First and Second order filters. (9)

DIGITAL TO ANALOG & ANALOG TO DIGITAL CONVERTERS: Non-idealities in the DAC - Types of DAC's: Current switched, Resistive, Charge redistribution (capacitive), Hybrid, segmented DAC's - Techniques for improving linearity - Analog to Digital Converters: quantization errors - non-idealities - types of ADC's: Flash, two step, pipelined, successive approximation, folding ADC's. (9)

SIGMA DELTA CONVERTERS: Over sampled converters - over sampling with out noise & with noise - implementation imperfections - first order modulator - decimation filters - second order modulator - sigma delta DAC & ADC's. (8)

ANALOG AND MIXED SIGNAL EXTENSIONS TO HDL: Introduction - Language design objectives - Theory of differential algebraic equations - the 1076 .1 Language - Tolerance groups - Conservative systems - Time and the simulation cycle - A/D and D/A Interaction - Quiescent Point - Frequency domain modeling and examples-analog extensions to Verilog**:** Introduction - data types –Expressions – Signals- Analog behavior –Hierarchical Structures –Mixed signal Interaction. (10)

Total L: 45

REFERENCES:

1. David A Johns and Ken Martin, "Analog Integrated Circuit Design", John Wiley and Sons, 2008.
2. Rudy van de Plassche, "Integrated Analog-to-Digital and Digital-to-Analog Converters", Kluwer, 2007.
3. Antoniou, "Digital Filters Analysis and Design", Tata McGraw Hill, 2007.
4. Phillip Allen and Douglas Holberg "CMOS Analog Circuit Design", Oxford University Press, 2012.
5. Benhard Razavi, "Data Converters", Kluwer Publishers, 2005.
6. Jacob Baker, Harry W Li, and David E Boyce "CMOS, Circuit Design Layout and Simulation", Wiley- IEEE Press, 1998.
7. Tsividis Y P, "Mixed Analog and Digital VLSI Devices and Technology", Mc-Graw Hill, 2002.
8. Jacob Baker, "CMOS, Circuit Design Layout and Simulation", Wiley- IEEE Press, 2011.
9. Rolf Schaumann and Mac E Van Valkenburg, "Design of Analog Filters", Oxford University Press, 2003.

10. Kenneth S Kundert and Olaf Zinke, “The Designers Guide to Verilog AMS”, Kluwer Publications, 2004.

15LV22 HARDWARE VERIFICATION TECHNIQUES

3 0 0 3

VERIFICATION TECHNOLOGIES AND TOOLS : Importance of Verification - Reconvergence Model - The Human Factor - Formal and Functional Verification Approaches - Timing Verification - Testing Versus Verification - Design and Verification Reuse - Linting - Simulation - Third Party Models - Verification Intellectual Property - Waveform Viewers - Code Coverage - Functional Coverage - Issue Tracking – Metrics - Role of the Verification Plan - Levels of Verification - Verification Strategies. (10)

HIGH-LEVEL MODELING : High-Level Versus RTL Thinking - Structure of High-Level Code - Data Abstraction - Object-Oriented Programming - Parallel Simulation Engine - Race Conditions - Portability Issues. (9)

STIMULUS AND RESPONSE: Simple Stimulus - Simple Output - Complex Stimulus - Bus-Functional Models - Response Monitors - Transaction Level Interface. (9)

ARCHITECTING TESTBENCHES AND SIMULATION MANAGEMENT: Verification Harness - Design Configuration - Self-Checking Test benches - Directed Stimulus - Random Stimulus - System Level Verification Harnesses - Transaction Level Models - Managing Simulations - Regression. (9)

VERIFICATION METHODOLOGY: Universal Verification Methodology (UVM) – Packages – Components – Environmental Structure – Factory Registration – Reporting. (8)

Total L: 45

REFERNCES:

1. Janick Bergeron, “Writing Test Benches Using System Verilog”, Springer, 2009.
2. Chris Spear, Greg Tumbush, "System Verilog for Verification - A Guide to Learning the Testbench Language Features" Springer, 2012.
3. Sharon Rosenberg and Kathleen Meade, "A Practical Guide to Adopting the Universal Verification Methodology (UVM)", Cadence Design Systems, Inc., 2013.
4. Andreas Meyer, “Principles of Functional Verification”, Newnes, 2003.
5. Kropf T, “Introduction to Formal Hardware Verification”, Springer Verlag, 2010.

15LV23 SEMICONDUCTOR MEMORY DESIGN AND TESTING

3 0 0 3

RANDOM ACCESS MEMORY TECHNOLOGIES: Static Random Access Memories (SRAM): SRAM cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral Circuit Operation, Bipolar SRAM Technologies, Silicon on insulator (SOI) Technology. Advanced SRAM Architectures and Technologies, Application Specific SRAMs. Dynamic Random Access Memories (DRAM): DRAM Technology Development, CMOS DRAM, DRAM cell theory and advanced cell structures, BiCMOS DRAM, soft error failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAM. (9)

NON-VOLATILE MEMORIES: Masked Read only Memories (ROM), High Density ROMs, Programmable ROM, Bipolar ROMs, CMOS PROMs, Erasable(UV) Programmable ROM(EPROM), Floating, Gate EPROM Cell, One time Programmable EPROM (OTPEPROM), Electrically Erasable PROMS, EEPROM Technology and Architecture, Non volatile SRAM, Flash Memories (EPROM or EEPROM), Advanced Flash Memory Architecture, Content Addressable Memory. (10)

MEMORY FAULT MODELLING TESTING AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE: RAM Fault Modeling, Electrical Testing, and Peusdo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing. Ram FAULT Modeling, BIST Techniques for Memory. (8)

SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS: General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification. Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures (9)

ADVANCED MEMORY TECHNOLOGIES AND HIGH-DENSITY MEMORY PACKAGING TECHNOLOGIES: Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories- Magnetoresistive Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions. (9)

Total L: 45

REFERENCES:

1. Ashok K Sharma, “Semiconductor Memories Technology, Testing and Reliability”, Wiley, 2002.
2. Ashok K Sharma, “Advanced Semiconductor Memories – Architecture, Design and Applications, Wiley, 2002.

3. Betty Prince, "Emerging Memories - Technologies and Trends", Kluwer Academic Publishers, 2002.
4. Kiyoo Itoh, Masashi Horiguchi and Hitoshi Tanaka, "Ultra-Low Voltage Nano-Scale Memories", Springer, 2007.
5. Jesse Russell and Ronald Cohn, "Content-Addressable Memory", Bookvika Publishing, 2012.

15LV24 VLSI TECHNOLOGY

3 0 0 3

MATERIAL PROPERTIES & CRYSTAL GROWTH: Crystal structure- axes & planes, Crystal defects-Point defects & dislocations Crystal growth- Bridgman, Czochralski techniques & Zone process, Doping in the melt. (8)

DIFFUSION & ION IMPLANTATION: Nature of diffusion-interstitial, Substitutional, interstitial substitutional movements, Diffusion constant, Dissociate process, Diffusion equation- D is constant & function, Diffusion systems, problems in Si Diffusion, Evaluation Techniques Ion Implantation: Penetration range, Implantation Damage, Annealing, Implantation Systems. (10)

OXIDATION & EPITAXY OXIDATION: Thermal Oxidation-Intrinsic, Extrinsic silicon Glass, Oxide formation, Kinetics of Oxide growth, Oxidation systems, Faults, Anodic Oxidation. EPITAXY: Vapour Phase Epitaxy (VPE)- transport, reaction and growth, Chemistry of growth, Insitu etching, Selective epitaxy, imperfections, Liquid Phase Epitaxy, LPE system, Evaluation of epitaxial layers. (9)

ETCHING & LITHOGRAPHY: LITHOGRAPHY: Pattern generation & Masking, Printing & Engraving-Optical, E-Beam, ion Beam, X-Ray, Photo resists, Defects. ETCHING: Wet chemical etching- anisotropic etchants, Etching for non-crystalline films-Plasma etching, Plasma-assisted etching, cleaning. (9)

DEVICE & CIRCUIT FABRICATION: Isolation- Mesa, Oxide, PN-junction isolations, Self Alignment, Local Oxidation, Planarisation, Metallisation and Packaging. Circuits – N, P and CMOS Transistors, Memory devices, BJT Circuits – Buried Layer, PNP and NPN Transistors, Diodes, Resistors, Capacitors. (9)

Total L: 45

REFERENCES:

1. Sorab K Gandhi, “VLSI Fabrication Principles – Silicon and Gallium Arsenide”, Wiley Interscience Publications, New York 2007.
2. Sze S M, “VLSI Technology”, McGraw Hill, New York, 2003.
3. Chang S Y and Sze S M, “ULSI Technology”, McGraw Hill, New York, 2007.
4. Groove A S, “Physics and Technology of Semiconductor Devices”, Wiley Interscience Publications, New York, 2007.
5. Sze S M and Kwok K Ng ,“Physics of Semiconductor Devices”, John Wiley , 2006

15LV25 RF CIRCUIT DESIGN

3 0 0 3

PASSIVE RF COMPONENTS AND TRANSMISSION LINE ANALYSIS: High frequency Resistors, Capacitor and Inductors – Transmission Line Analysis: Line equation, Micro strip line, Voltage Reflection Co-efficient, propagation constant phase velocity and special termination - Smith Chart-Impedance transformation - Analysis of parallel RL circuit and parallel RC circuit. (9)

SINGLE AND MULTI PORT NETWORK THEORY AND RF FILTER DESIGN: Definition - properties - interconnection of networks - ABCD parameters and S parameters - RF Filter Resonator and filter configuration - Butterworth and chebyshev filters. Design of micro strip filters. (9)

DESIGN OF MATCHING NETWORK: Matching by Discrete Components - Design of two-component matching network, Design of T and π matching network- Matching by micro strip line - Design of matching network - Design of stub matching. (9)

RF ACTIVE COMPONENTS, THEIR MODELING AND RF AMPLIFIER DESIGN: Components: RF Diode: PIN diode and Gunn Diode. RF Bipolar junction Transistor, RF field effect transistor - Modeling: Diode model, Transistor model, and FET model – RF Amplifier: Characteristics, power relations and Stability considerations. (9)

RF OSCILLATOR AND MIXER DESIGN: Basic oscillator model - Design of fixed frequency oscillator - Dielectric resonator oscillator - voltage controlled oscillator - gun element oscillator - Basic concepts - Design of single ended mixer- Double ended mixer. (9)

Total L: 45

REFERENCES:

1. Reinhold Ludwig and Pavel Bretchko, “RF Circuit Design”, Pearson Education Asia Publication, 2011.
2. Matthew M Radmanesh, “Radio Frequency and Microwave Electronics Illustrated”, Pearson Education, Asia Publication, 2001.
3. Peter P Kenington, “High Linearity RF Amplifier Design”, Artech House, 2007.
4. Razavi B, “RF Micro Electronics”, Prentice Hall PTR, 2011.
5. Lee T H, “The Design of CMOS Radio Frequency Integerated Circuits”, Cambridge University Press, 2004.

15LV26 VLSI FOR WIRELESS COMMUNICATION

3 0 0 3

OVERVIEW OF MODULATION SCHEMES: Classical Channel - Wireless Channel Description - Path Loss - Channel Model and Envelope Fading - Multipath Fading: Frequency Selective and Fast Fading - Summary of Standard Translation. (8)

RECEIVER FRONT END: Filter Design - Rest of Receiver Front End: Non idealities and Design Parameters - Nonlinearity –Noise - Derivation of Noise Figure. (8)

AMPLIFIER DESIGN: Low Noise Amplifier Design - Wideband LNA - Design Narrowband LNA - Impedance Matching - Automatic Gain Control Amplifiers – Power Amplifiers. (9)

MIXERS: Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion - Low Frequency Case: Analysis of Gilbert Mixer – Distortion - High-Frequency Case – Noise - A Complete Active Mixer. Switching Mixer - Distortion in Unbalanced Switching Mixer - Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer- Demodulators. (10)

FREQUENCY SYNTHESIZERS: Phase Locked Loops - Voltage Controlled Oscillators - Phase Detector – Analog Phase Detectors – Digital Phase Detectors - Frequency Dividers - LC Oscillators - Ring Oscillators - Phase Noise - A Complete Synthesizer Design Example (DECT Application). Loop filter**:** General Description - Design Approaches. (10)

Total L: 45

REFERENCES:

1. Bosco H Leung “VLSI for Wireless Communication”, Pearson Education, 2002.
2. Emad N Farag and Mohamed I Elmasry, “Mixed Signal VLSI Wireless Design - Circuits and Systems”, Kluwer Academic Publishers, 2000.
3. Iaskar J, Matinpourand B and Charaborty S, “Modern receiver front ends: Systems, Circuits and integration”, Wiley 2004
4. Leenearts D, Vander J Tang and Vaucher C S, “Circuit design for RF transceivers”, Springer 2002.
5. Luzzatto A and Shirazi G, “Wireless Transceiver Design: Mastering the Design of Modern Wireless Equipment and Systems”, Wiley 2007.

15LV27 SYSTEM LEVEL HARDWARE SOFTWARE CO-DESIGN

3 0 0 3

CO-DESIGN CONCEPTS: Nature of hardware & software, quest for energy efficiency, driving factors for hardware-software co design, design space, system specification and modelling- Embedded systems-Functional decomposition, Hardware Software tradeoffs- Comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification. (8)

METHODOLOGY FOR CO-DESIGN: partitioning source description into different implementation domains, Dataflow modeling and transformation, Dataflow implementation in Hardware and Software, Analysis of Control flow and Dataflow, hardware-software co-synthesis, Distributed System Co-Synthesis. (10)

HARDWARE-SOFTWARE INTEGRATION: Prototyping and Emulation Techniques, Target Architectures-Micro programmed Architectures, General-Purpose Embedded Cores, System-on-Chip, Hardware-Software Interfaces, Principles of Hardware/Software Communication, Microprocessor Interfaces, Hardware Interfaces. (10)

OBJECTED ORIENTED HARDWARE DESIGN: Motivation for object oriented techniques, object oriented design strategies, modelling hardware components as classes, designing specialized components, data decomposition, and Processor example. (8)

SYSTEM C PROGRAMMING: Design Methodology, Modules and Hierarchy, Processes, Ports and signals, Data types, Simulation using SystemC. CASE STUDY: Processor/Coprocessor design using SystemC. (9)

Total L: 45

REFERENCES:

1. Patrick Schaumont “A Practical Introduction to Hardware/Software Co-design”, Patrick Schaumont, Springer, 2012.
2. Ralf Niemann, “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer, 1998.
3. Alxel Jantsch, “Modeling Embedded Systems and SOC’s. Concurrency and Time in Models of Computation”, MK, 2004.
4. Vahid and Frank, “Embedded System Design: A Unified Hardware/Software Introduction”, Wiley, 2002.
5. Wolf and Wayne, “Computers as Components: Principles of Embedded Computing System Design”, MK, 2001.
6. Grotker T, Liao S, Martin G and Swan S, “System design with SystemC”, Kluwer Academic Publishers, 2002.

15LV28 SYSTEM ON CHIP DESIGN

3 0 0 3

INTRODUCTION TO THE CONCEPT OF SoC: Driving Forces for SoC - Components of SoC - Design flow of SoC - Hardware/Software nature of SoC - Design Trade-offs - SoC Applications - SYSTEM-LEVEL DESIGN: Processor selection- Concepts in Processor Architecture: Instruction set architecture (ISA), elements in Instruction Handing-Robust processors: Vector processor, VLIW, Superscalar, CISC, RISC—Processor evolution: Soft and Firm processors, Custom-Designed processors- on-chip memory. (10)

SYSTEM-LEVEL INTERCONNECTION: On-chip Buses: basic architecture, topologies, arbitration and protocols, Bus standards: AMBA, CoreConnect, Wishbone, Avalon - Network-on-chip: Architecture-topologies-switching strategies - routing algorithms - flow control, Quality-of-Service- Reconfigurability in communication architectures. (8)

IP BASED SYSTEM DESIGN: Introduction to IP Based design, Types of IP, IP across design hierarchy, IP life cycle, Creating and using IP - Technical concerns on IP reuse - IP integration - IP evaluation on FPGA prototypes. (10)

SOC IMPLEMENTATION: Study of processor IP, Memory IP, wrapper Design - Real-time operating system (RTOS), Peripheral interface and components, High-density FPGAs - EDA tools used for SOC design. (9)

SOC TESTING: Manufacturing test of SoC: Core layer, system layer, application layer-P1500 Wrapper Standardization-SoC Test Automation (STAT). (8)

Total L: 45

REFERENCES:

1. Michael J Flynn and Wayne Luk, “Computer system Design: System-on-Chip”, Wiley-India, 2012.
2. Sudeep Pasricha and Nikil Dutt, “On Chip Communication Architectures: System on Chip Interconnect”, Morghan Kaufmann Publishers, 2008.
3. Wolf W H, “Computers as Components: Principles of Embedded Computing System Design”, Elsevier, 2008.
4. Patrick Schaumont “A Practical Introduction to Hardware/Software Co-design”, Patrick Schaumont, Springer, 2012.
5. Lin, Y-L S (ed.), “Essential Issues in SOC Design: Designing Complex Systems-on-chip. Springer, 2006.
6. Wayne Wolf, “Modern VLSI Design: IP Based Design”, Prentice-Hall India, 2009.

15LV29 SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS

3 0 0 3

INTRODUCTION: Boolean functions, satisfiability and cover. Abstract models, state diagrams. Data flow and sequencing graphs, compilation and behavioural optimization. (8)

ARCHITECTURAL SYNTHESIS: Circuit specifications for architectural synthesis. Temporal domain, spatial domain, hierarchical models. Synchronization problems. Area and performance estimation. Strategies for architectural optimization, Data path synthesis of pipelined circuits. (10)

SCHEDULING ALGORITHMS: Scheduling with and without constraints. Scheduling algorithms for extended sequencing models. Scheduling pipelined circuits. (8)

RESOURCE SHARING AND BINDING: Sharing and binding for resource dominated circuits and general circuits. Concurrent binding and scheduling. Resource sharing and binding for non-scheduled sequencing graphs. (9)

SEQUENTIAL LOGIC OPTIMIZATION:sequential circuit optimization using state based models and network models. Implicit finite state machine. Traversal methods. Testability considerations for synchronous circuits. (10)

Total L: 45

REFERENCES:

1. De Micheli G, “Synthesis and optimization of Digital circuits”, McGraw Hill, 1994.
2. Philippe Coussy and Adam, “High Level Synthesis: From Algorithm to Digital Circuit”, Springer, 2008.
3. Mohanthy S P, Ranganathan N and Kougianos E, “Low Power High Level Synthesis for Nanoscale CMOS Circuits” , Springer, 2008.
4. Aarto P, Visegrady T and Jankovits I, “High Level Synthesis of Pipelined Data Paths”, Wiley, 2001.

15LV30 HIGH SPEED DIGITAL DESIGN

3 0 0 3

TRANSMISSION LINES AND CROSSTALK: Transmission line structures, signal propagation, transmission line parameters, line impedance, propagation delay, Transmission line reflections, Cross talk- Mutual inductance, Mutual capacitance, cross talk induced noise, minimizing cross talk. (10)

INTERCONNECTS: Interconnect technologies, multilevel multilayer interconnects, propagation delay, crosstalk analysis. (8)

POWER DISTRIBUTION: losses, the need for low-impedance planes and decoupling capacitors and their selection. (9)

CLOCK DISTRIBUTION AND TIMING: High-quality clock signals to components, boards, and systems, Common clock timing and source synchronous timing. (9)

ELECTROMAGNETIC COMPATIBILITY (EMC): Designing for EMC, EMC regulations, typical noise path, methods of noise coupling, and methods of reducing interference in systems. grounding**:** Safety grounds ,signal grounds, single-point ground systems, multi-point ground systems, hybrid grounds, functional ground layout, practical low frequency grounding, hardware grounds, grounding of cable shields, ground loops, shield grounding at high frequencies. (9)

Total L: 45

REFERENCES:

1. Howard Johnson and Martin Graham, “High speed Digital design”, Pearson, 2005.
2. Hall S, Hall G and McCall J, “High Speed Digital System Design: A Handbook of Interconnect Theory and Practices”, Wiley Interscience, 2000.
3. Hartmut Grabinski, “Interconnects in VLSI design”, Kluwer, 2000.
4. Goel A K, “High Speed Vlsi Interconnections”, Wiley, 2007.
5. Bogatin E, “Signal Integrity-Simplified”, Prentice Hall, 2003.
6. Paul C R, “Introduction to Electromagnetic Compatability”, Wiley, 2006.

15LV31 MICROSENSORS AND MEMS

3 0 0 3

OVERVIEW OF MICRO SENSORS AND MEMS: Introduction –MEMS and micro system products- Microsystems and Microelectronics -Applications of micro systems in automotive industry and in other industries. (8)

MATERIALS FOR MEMS AND MICRO SENSORS: Silicon-silicon compounds-silicon piezo resistors-gallium arsenide-quartz-piezoelectric crystals-polymers-packaging materials. (9)

MICROSYSTEM DESIGN: Design considerations-design constraints-selection of materials-manufacturing process, signal transduction-packaging. (9)

PROCESS DESIGN-photolithography, thin film fabrications, geometry shaping - mechanical design-design of silicon die for micro pressure sensor. (9)

MICRO SENSORS: Introduction- micro sensors- biomedical sensors-pressure sensors-thermal sensors-chemical sensors-optical sensors-micro actuation –mems with micro actuators. (10)

Total L: 45

REFERENCES:

1. Tai-Ran Hsu, “MEMS and Microsystems Design and Manufacture”, Tata McGraw-Hill, 2002.
2. John A Pelesko, “Modeling MEMs and NEMS”, CRC press, 2002.

15LV32 NANO SCALE DEVICES

3 0 0 3

OVERVIEW: Nano devices, Nano materials, Nano characterization-Definition of Technology node. Basic CMOS Process flow- MOS Scaling theory, Issues in scaling. MOS transistors: Short channel effects, Description of a typical 65 nm CMOS technology-Requirements for Non classical MOS transistor. MOS CAPACITOR: Role of interface quality and related process techniques, Gate oxide thickness scaling trend, SiO2 vs High-k gate dielectrics- Integration issues of high-k -Interface states, bulk charge, band offset, stability, reliability - Q_{bd} high field, possible candidates, CV and IV techniques. (10)

METAL GATE TRANSISTOR : Motivation, requirements, Integration Issues- Transport in Nano MOSFET, velocity saturation, ballistic transport, injection velocity, velocity overshoot - Ultrathin body SOI - double gate transistors, integration issues - Vertical transistors - FinFET and Surround gate FET. (11)

METAL SOURCE/DRAIN JUNCTIONS: Properties of schotky junctions on Silicon, Germanium and compound semiconductors - Work function pinning- Germanium Nano MOSFETs: strain, quantization, Advantages of Germanium over Silicon, PMOS versus NMOS. Compound semiconductors - material properties, MESFETs Compound semiconductors MOSFETs in the context of channel quantization and strain, Hetero structure MOSFETs exploiting novel materials, strain, and quantization. (10)

SYNTHESIS OF NANOMATERIALS: CVD, Nucleation and Growth, ALD, Epitaxy, MBE. Compound semiconductor hetero-structure growth and characterization - Quantum wells and Thickness measurement techniques - Contact - step height, Optical - reflectance and ellipsometry.AFM. Characterization techniques for nanomaterials: FTIR, XRD, AFM, SEM, TEM, EDAX etc-Applications and interpretation of results. (11)

EMERGING NANO MATERIALS : Nanotubes, nanorods and other nano structures, LB technique, Soft lithography etc. Microwave assisted synthesis, Self assembly etc. (3)

Total L: 45

REFERENCES:

1. Karl Goser, Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices, Springer, 2005.
2. Waser Ranier, "Nanoelectronics and Information Technology (Advanced Electronic Materials and Novel Devices", Wiley-VCH, 2005.

15LV33 ADVANCED COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

3 0 0 3

INTRODUCTION TO PARALLEL PROCESSING: - Evolution of computer systems. Generation of computer systems – Trends towards parallel processing- Parallel processing mechanisms- parallel computer structure- Architectural classification schemes – Application. (8)

MEMORY AND I/O SUBSYSTEMS, PIPELINING: Hierarchical Memory structure – Virtual memory system - cache memory management- Memory allocation and management – I/O subsystems **pipelining:** Principles - Classification of pipeline processors - Reservation tables – Interleaved memory organization – Design of arithmetic pipeline – Design of instruction pipeline. (10)

VECTOR AND ARRAY PROCESSING: Need – Basic vector processing architecture - Issues in vector processing – Vectorization and optimization methods. Array processing**:** SIMD Array processors – SIMD interconnection networks – Parallel algorithms for array processors – associative array processing. (9)

MULTIPROCESSOR ARCHITECTURE: Functional structures - Interconnection network – Multi cache problems and solutions – Exploiting concurrency for multiprocessing. (9)

PRINCIPLES OF PARALLEL ALGORITHM DESIGN: Design approaches-Design issues-Performance measures and analysis-Complexities-Anomalies in parallel algorithms - Pseudo code conventions for parallel algorithms-Comparison of SIMD and MIMD algorithms. (9)

Total L: 45

REFERENCES:

1. Kai Hwang, "Advanced Computer Architecture: Parallelism, Scalability and Programmability", Tata McGraw Hill, 1992.
2. Seyed Roosta, "Parallel Processing and Parallel Algorithms", Springer Series, 2000.
3. John L Hennessy, "Computer Architecture a Quantitative Approach", Harcourt Asia Pvt. Ltd., 2011.

15LV34 BIOMEDICAL SIGNAL PROCESSING

3 0 0 3

INTRODUCTION TO BIOMEDICAL SIGNALS: Examples of Biomedical signals - ECG, EEG, and EMG etc - Tasks in Biomedical Signal Processing - Computer Aided Diagnosis. Origin of bio potentials - Review of linear systems – Processing of Random & Stochastic signals-Modeling Stochastic signals as filtered White Noise-Nonlinear models of signals- Properties and effects of noise in biomedical instruments - Filtering in biomedical instruments. (9)

CASE STUDIES ON CONCURRENT, COUPLED AND CORRELATED PROCESSES: Adaptive and optimal filtering – Random noise, structured noise and physiological interference—Filtering for removal of artifacts -Maternal interference in Fetal ECG - Muscle-contraction interference. Event detection - case studies with ECG & EEG – correlation analysis of EEG channels. (9)

CARDIO VASCULAR APPLICATIONS: Basic ECG - Electrical Activity of the heart- ECG data acquisition – ECG parameters & their estimation - Use of multiscale analysis for ECG parameters estimation – Arrhythmia analysis. (9)

ECG Signal Processing: Baseline Wandering, Power line interference, Muscle noise filtering - Data Compression: Direct Data Compression Techniques-Direct ECG Data Compression Techniques. (9)

NEUROLOGICAL APPLICATIONS: Electroencephalogram - EEG rhythms & waveform - categorization of EEG activity - recording techniques - EEG Analysis- EEG applications- Epilepsy, sleep EEG-Data acquisition and classification of sleep stages- EEG segmentation-Fixed Segmentation-Adaptive segmentation- coherence analysis of EEG channels. (9)

Total L: 45

REFERENCES:

1. Rangaraj M. Rangayyan, "Biomedical Signal Analysis", Wiley, 2012.
2. Reddy D C, "Biomedical Signal Processing: Principles and techniques", Tata McGraw Hill, New Delhi, 2005.
3. Bruce, "Biomedical Signal Processing & Signal Modeling," Wiley, 2001.
4. Enderle, "Introduction to Biomedical Engineering," 2/e, Elsevier, 2005.

15LV35 GENETIC ALGORITHMS FOR VLSI DESIGN

3 0 0 3

INTRODUCTION: GA Terminology-steady state algorithm-Genetic Operators-Partitioning-circuit partitioning by genetic algorithm-Hybrid Genetic algorithm for Ratio-cut portioning. (9)

GA FOR PLACEMENT AND ROUTING: standard cell placement-Macro cell placement-Macro cell Routing-Steiner problem in graph-Macro cell Global Routing. (9)

FPGA TECHNOLOGY MAPPING: Circuit segmentation and FPGA mapping-circuit segmentation for Pseudo-Exhaustive testing. (8)

AUTOMATIC TEST GENERATION: Test generation in a GA framework-Test generation for test application Time Reduction-Deterministic/Genetic Test generator Hybrids-use of FSM sequences. (10)

PEAK POWER ESTIMATION: Application of Genetic algorithms to peak power estimation-Estimation of peak single-cycle and n-cycle powers-Peak Sustainable power estimation. (9)

Total L: 45

REFERENCES:

1. Pinaki Mazumder, E MRudnick, "Genetic Algorithm for VLSI Design, Layout and test Automation", Prentice Hall, 1998.
2. Randy L Haupt, Sue Ellen Haupt, "Practical Genetic Algorithms", Wiley-Interscience, 1977.
3. Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B R Vellasco and Marley Maria Bernard Vellasco, "Evolution Electronics: Automatic Design of Electronic Circuits and Systems Genetic Algorithms", CRC press, 2001.
4. John R Koza, Forrest H Bennett III, David Andre and Morgan Kufmann, "Genetic Automatic Programming and Circuit Synthesis", 1999.

15LV36 VLSI FOR BIOMEDICAL APPLICATIONS

3 0 0 3

LOW-POWER ANALOG AND BIOMEDICAL CIRCUITS: Low power transimpedance amplifiers and photoreceptors- Low power transconductance amplifiers and scaling laws for power in analog circuits- Low-power filters and resonators- Low power current-mode circuits - Ultra-low-power and neuron-inspired analog-to-digital conversion for biomedical system. (10)

LOW-POWER RF AND ENERGY-HARVESTING CIRCUITS FOR BIOMEDICAL SYSTEMS: Wireless inductive power links for medical implants - Energy-harvesting RF antenna power links - Low-power RF telemetry in biomedical implants. (8)

BIOMEDICAL ELECTRONIC SYSTEMS : Ultra-low-power implantable medical electronics- cochlear implants or bionic ears-an ultra low power programmable analog bionic ear processor-low power electrode stimulation-highly miniature electrode –stimulation – Brain machine interfaces for the blind-Brain machine interface for paralysis, speech, and other disorders. Ultra-low-power noninvasive medical electronics -Analog integrated-circuit switched-capacitor model of the heart – the electrocardiogram- A micro power electrocardiogram amplifier -Low-power pulse oximetry - Battery-free tags for body sensor networks -Intra-body galvanic communication networks - Biomolecular sensing. (10)

PRINCIPLES FOR ULTRA-LOW-POWER ANALOG AND DIGITAL DESIGN: digital design- Sizing and topologies for robust sub threshold operation-Types of power dissipation-energy efficiency-Optimization of energy efficiency-Varying the power-supply voltage and threshold voltage-gated clocks-Basics of adiabatic computing-adiabatic clocks- Architectures and algorithms for improving energy efficiency. Analog and mixed-signal design -Power consumption in analog and digital systems-low power hand- The optimum point for digitization in mixed-signal system Common themes in low-power analog and digital design-The Shannon limit for energy efficiency-Collective analog or hybrid computation-HSMs: general-purpose mixed-signal systems with feedback-General principles for low-power mixed-signal system design-The evolution of low-power design-Actuators and sensors. (9)

BIO-INSPIRED SYSTEMS: Neuromorphic electronics- Transmission-line theory- The cochlea: biology, motivations, theory, and RF-cochlea design- A bio-inspired analog vocal tract- Bio-inspired vision architectures Hybrid analog-digital computation in the

brain- Spike-based hybrid computers- Energy efficiency in neurobiological systems Cytomorphic electronics: cell-inspired electronics for systems and synthetic biology- Electronic analogies of chemical reactions- Log-domain current-mode models of chemical reactions and protein-protein networks- Analog circuit models of gene-protein dynamics- Logic-like operations in gene-protein circuits- Circuits-and-feedback techniques for systems and synthetic biology- Hybrid analog-digital computation in cells and neurons. (8)

Total L: 45

REFERENCES:

1. Rahul Sarpeshkar, "Ultra Low Power Bioelectronics: Fundamentals, Biomedical Applications, and Bio-Inspired Systems" Cambridge University Press, 2011
2. Kris Iniewski, "VLSI Circuit Design for Biomedical Applications", Artech House Publishers, 2008.

15LV37 HARDWARE SECURITY

3 0 0 3

HARDWARE IMPLEMENTATION OF CRYPTOGRAPHIC ALGORITHMS: Introduction - Need for hardware security – Basics and vulnerabilities - Design for security - Mathematical Background - Modular Arithmetic - Finite Field - Hardware Implementation of Public-key Cryptographic Algorithm - Private-key Cryptographic Algorithm - Stream Ciphers - Hash Functions. (10)

SIDE CHANNEL ANALYSIS: Introduction - Power Analysis Attack - Timing Attack - Fault Attack - Cache Attack – Scan Chain Based Attack - Design Techniques To Prevent Side Channel Analysis Attacks. (9)

HARDWARE TROJANS: Overview - Nomenclature and Operating Modes - Hardware Trojan Detection Techniques - Logic Testing - Countermeasures - Design Technique - Manufacturing Technique. (9)

PHYSICALLY UNCLONABLE FUNCTIONS: Introduction – Design Approaches - Modeling of PUFs - Sources of Mismatch and Errors - Testing of PUFs - Practical Realizations - Applications. (8)

COUNTERFEIT ICs: Taxonomies - Assessment - Challenges - Detection and Prevention of Recycled ICs - Path Delay Fingerprinting – Secure Hardware Intellectual Properties: - Need for IP protection - Digital Watermarking - Constraint-based Watermarking to Design IP Protection - Watermarking HDL Source Codes by Duplicating Modules. (9)

Total L: 45

REFERENCES:

1. Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, "Hardware Security - Design, Threats, and Safeguards", CRC Press, 2015.
2. Mohammad Tehranipoor, Hassan Salmani and Xuehui Zhang, "Integrated Circuit Authentication Hardware Trojans and Counterfeit Detection", Springer, 2014.
3. Mohammad Tehranipoor and Cliff Wang, "Introduction to Hardware Security and Trust", Springer, 2012.
4. Christoph Bohm and Maximilian Hofer, "Physical Unclonable Functions in Theory and Practice", Springer, 2013.
5. Rodriguez-Henriquez F, Saqib N A, Díaz Pérez A and Koc K C, "Cryptographic Algorithms on Reconfigurable Hardware", Springer, 2007.
6. Koc K C, "Cryptographic Engineering", Springer, 2009.

15LV38 NETWORK ON CHIP

3 0 0 3

INTRODUCTION AND MOTIVATION: SoC objectives and NoC needs, State of the art Taxonomy, Technology trends, Characteristics of NoCs, Component design for NoCs, Properties of network architectures. (8)

ARCHITECTURES FOR NOCS: Shared medium networks, direct networks, indirect networks, Hybrid networks, Standard architectures and formal properties, Network architectures for on-chip realization, Ad hoc network architectures. (9)

PHYSICAL NETWORK AND DATA-LINK LAYER: Wiring issues, Physical routing, Signaling, Driver/receiver design, Noise immunity, Shielding, Medium access control, Data encoding, Error correcting codes: theory and practice, Arbitration issues. (10)

NETWORK AND TRANSPORT LAYERS: Packets, Flits, Switching techniques, No topologies, Routing algorithms and routers, QoS guarantees, Congestion and Flow control. (9)

SOFTWARE AND TOOLS FOR NOCs: Programming paradigms- shared medium vs. message passing, Middleware issues-layering and software encapsulation, Application layer issue and network-aware compilation, Analysis and Synthesis of NoCs, Present tools (Bones, Xpipes) and future outlook. (9)

Total L: 45

REFERENCES:

1. Giovanni De Micheli and Luca Benini “Networks on Chips: Technology and Tools”, Academic Press, 2006.
2. Axel Jantsch, Hannu Tenhunen “Networks on Chips”, Springer, 2003.
3. Davide Bertozzi, Shashi Kumar, Maurizio Palesi “Networks on Chips”, Hindawi Publishing Corporation, 2007.

15LV39 ELECTRONIC PACKAGING TECHNOLOGIES

3 0 0 3

OVERVIEW OF ELECTRONIC SYSTEMS PACKAGING: Packaged Electronics – Technologies- Trends- Products and levels of packaging- Packaging aspects of handheld products. (9)

SEMICONDUCTOR PACKAGING OVERVIEW: Basics of Semiconductor and Process flowchart; Wafer packaging; Packaging evolution- Chip connection choices -Wire bonding, TAB and flipchip. (9)

SEMICONDUCTOR PACKAGES: Single chip packages or modules (SCM)-. Commonly used packages and advanced packages; Materials in packages- Advances packages Thermal mismatch in packages; Current trends in packaging- Multichip modules (MCM)-types; System-in package(SIP)- Packaging roadmaps- Hybrid circuits. (9)

ELECTRICAL DESIGN CONSIDERATIONS IN SYSTEMS PACKAGING: Electrical Issues – Resistive Parasitic - Capacitive and Inductive Parasitic- Layout guidelines and the Reflection problem-Interconnection. (9)

THERMAL MANAGEMENT AND RELIABILITY: Heat-transfer fundamentals-. Thermal conductivity and resistance- Conduction, convection and radiation- Cooling –Reliability- Basic concepts- Environmental interactions- Thermal mismatch and fatigue. (9)

Total L: 45

REFERENCES:

1. Rao R Tummala, “Fundamentals of Microsystems Packaging”, McGraw Hill, NY, 2001.
2. William D Brown, “Advanced Electronic Packaging”, IEEE Press, 1999.

15LV44 MODELING AND SIMULATION OF NANOSCALE TRANSISTORS

2 2 0 3

ANALYTICAL MODELING: Introduction -Types of Models - Attributes of Good Compact Models - Model Formulation - Model Implementation in Circuit Simulators - Model Testing - Parameter Extraction - Simulation and Extraction for RF Applications. Analytical Solution Methods: Parabolic Approximation - Variable Separable - Numerical Simulation - Fourier series - Green Function - Bessel Function. (7+4)

TECHNOLOGY-ORIENTED CAD: Introduction – Process and Device CAD – Process Simulation Techniques – Interfaces in process and Device CAD – CMOS Technology - Ion Implantation – Oxidation – Impurity Diffusion. (5+6)

DEVICE CAD: Semiconductor Device Analysis – The pn Junction – Equilibrium Conditions – Non-equilibrium Conditions - Bipolar Junction Structures - Carrier Densities – Carrier Transport and Conversation - Field-Effect Structures —The MOS capacitor – Basic MOSFET I-V Characteristics – Threshold Voltage in Nonuniform Substrate – MOS Device Design by Simulation. (5+6)

TCAD SIMULATION: Process simulator – Device simulator – Advanced concepts – drift-diffusion,hydrodynamic model, stress models - Structure editor - meshing concepts - work bench – Plotting – Scripting -Monte-carlo simulation - Electromagnetic simulation. (5+6)

NOVEL TRANSISTOR ARCHITECTURES: Nanowire transistor - High electron mobility transistor - Tunnel field effect transistor - Single electron transistor - Carbon nanotube transistor - Double gate and multi gate MOS transistor - Electron wave transistor - Electron spin transistor. (8+8)

Total: L: 30, T: 30

REFERENCES:

1. YannisTsividis and Colin McAndrew, "Operation and Modeling of the MOS Transistor", 3rd Edition, Oxford University Press, 2011.
2. Mark S. Lundstrom and Jing Guo, "Nanoscale Transistors: Device Physics, Modeling and Simulation", Springer, 2006.
3. Shunri Oda and David Ferry, “Silicon Nanoelectronics”, CRC Press, New York, 2005.
4. Robert W.Dutton and Zhiping Yu, “Technology CAD Computer Simulation of Processes and Devices”, Springer, 2012.
5.. Rainer Waser, “Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices”, 3rd Edition, Wiley VchVerlag, Weiheim, 2012.

15LV40/15LW48/15LC49 FPGA BASED IMPLEMENTATION OF SIGNAL PROCESSING SYSTEMS

3 2 0 4

FUNDAMENTALS OF FPGAs and DSP: Introduction to Field-programmable Gate Arrays, A Short History of the Microchip, Influence of Programmability, Challenges of FPGAs, DSP System Basics, DSP System Definitions, DSP Transforms, Filter Structures, Adaptive Filtering, Basics of Adaptive Filtering, Number Systems, Fixed-point and Floating-point, Arithmetic Operations, Fixed-point versus Floating-point. (9+6)

FPGA TECHNOLOGIES AND IMPLEMENTATION ISSUES: Xilinx FPGA Technologies, Altera FPGA Technologies, Various Forms of the LUT, Memory Availability Fixed Coefficient Design Techniques, Distributed Arithmetic, Reduced Coefficient Multiplier. (9+6)

ARCHITECTURES AND TOOLS FOR FPGA BASED DSP SYSTEMS: The Evolution of FPGA System Design, Design Methodology Requirements for FPGA DSP, System Specification, IP Core Generation Tools for FPGA, System-level Design Tools for FPGA, DSP Algorithm Characteristics, DSP Algorithm Representations, Basics of Mapping DSP Systems onto FPGAs, Parallel Operation, Hardware Sharing, Application to FPGA. (9+6)

COMPLEX DSP SYSTEMS: Motivation for Design for Reuse, Intellectual Property (IP) Cores, Evolution of IP Cores, Parameterizable (Soft) IP Cores, IP Core Integration, IP Core Example, Current FPGA-based IP Cores, Dataflow Modeling and Rapid Implementation for FPGA DSP Systems, System-level Design and Exploration of Dedicated Hardware. (9+6)

LOW POWER FPGA IMPLEMENTATION: Sources of Power Consumption, Power Consumption Reduction Techniques, Voltage Scaling in FPGAs, Reduction in Switched Capacitance, Data Reordering, Fixed Coefficient Operation, Pipelining, Locality, Application to an FFT Implementation, Reconfigurable Systems, Memory Architectures, Support for Floating-point Arithmetic. (9+6)

Total L: 45 + T: 30 = 75

TUTORIAL COMPONENT:

1. FPGA implementation of Digital Filters.
2. FPGA implementation Adaptive Filters.
3. FPGA implementation of Fixed point and Floating point Architectures.
4. FPGA implementation of Distributed Arithmetic Architecture.
5. IP Core Generation for System Level Design.
6. FPGA based DSP System implementation.
7. FPGA implantation of Reconfigurable systems.

REFERENCES:

1. Roger Woods, John McAllister, Gaye Lightbody and Ying Yi, “FPGA-based Implementation of Signal Processing Systems”, John Wiley and Sons, 2008.
2. Uwe Meyer Baese, “Digital Signal Processing with Field Programmable Gate Arrays”, Springer, 2004.
3. Wayne Wolf, “FPGA-Based System Design”, Prentice Hall, New Delhi, 2012.

15LV41/15LW46/15LC46 RF CIRCUITS AND MEASUREMENTS

3 2 0 4

PASSIVE RF COMPONENTS AND TRANSMISSION LINE ANALYSIS: High frequency Resistors, Capacitor and Inductors – Transmission Line Analysis: Line equation, Micro strip line, Voltage Reflection Co-efficient, propagation constant phase velocity and special termination - Smith Chart-Impedance transformation - Analysis of parallel RL circuit and parallel RC circuit. (9+6)

SINGLE AND MULTI PORT NETWORK THEORY AND RF FILTER DESIGN: Definition - properties - interconnection of networks - ABCD parameters and S parameters - RF Filter Resonator and filter configuration - Butterworth and chebyshev filters. Design of micro strip filters. (9+6)

DESIGN OF MATCHING NETWORK: Matching by Discrete Components - Design of two-component matching network, Design of T and π matching network- Matching by micro strip line - Design of matching network - Design of stub matching. (9+6)

MEASUREMENTS USING VECTOR NETWORK ANALYZER: Operating principles of VNA-Calibration of VNA- Specification of N and SMA connectors-Inferences of VNA Measurements. (9+6)

MEASUREMENTS USING SPECTRUM ANALYZER: Operating principles of spectrum analyzer- measurement categories-Characteristics of Spectrum analyzer-applications of spectrum analyzer. (9+6)

LAB COMPONENT: Design, simulation, fabrication and testing of any one of RF passive circuits. (Couplers, filters.)

Total L: 45 + T: 30 = 75

TUTORIAL COMPONENT:

1. Design, simulation and testing of branch-line coupler.
2. Design, simulation and testing of Rat-race coupler.
3. Design, simulation and testing of stepped impedance filter.
4. Design, simulation and testing of microstrip filter.

REFERENCES:

1. Reinhold Ludwig and Pavel Bretchko, "RF Circuit Design", Pearson Education Asia Publication, 2011.
2. Matthew M Radmanesh, "Radio Frequency and Microwave Electronics Illustrated", Pearson Education, Asia Publication, 2001.
3. David M Pozar, "Microwave Engineering", John Wiley and Sons, Inc., 2011.
4. Les Besser and Rowan Gilmore, "Practical RF Circuit Design for Modern Wireless Systems", Vol I, Passive Circuit and Systems, Artech house, London, 2003.

15LV42/15LW45/15LC47/ WIRELESS TECHNOLOGIES AND MEASURING TOOLS

3 2 0 4

MODERN WIRELESS COMMUNICATION SYSTEMS: Second Generation, Third Generation mobile Cellular networks – 4G, 5G, LTE, LTE A- Cognitive Radio Technology. (9+6)

RF SIGNAL AND SYSTEM FUNDAMENTALS: Basics of RF and Microwaves - Scattering parameters – Distribution of power – Deterministic & Random signal Power spectral densities – Microwave passive devices –Mixers – Switches – Attenuators – Connectors & adaptors. (9+6)

RF SIGNAL GENERATION: Oscillator Circuits – Direct Digital synthesis – PLL Based Synthesizers – Arbitrary waveform generator – Vector Signal Generator - Phase frequency detector. (9+6)

POWER AND SCATTERING MEASUREMENTS: Power detectors and instrumentation – Primary power standards – power measurement techniques – History of vector network analyzers – Measurement types in VNA – Two port network analyzer calibration. (9+6)

RF MODULAR INSTRUMENTS: Introduction – Understanding software designed systems – Multichannel measurements – Customized measurement systems – Instruments: Spectrum/Signal Analyser – Digital storage Oscilloscope - Mixed signal Oscilloscopes. (9+6)

Total L: 45 + T: 30 = 75

TUTORIAL COMPONENT:
1. Study of Vector Signal analysis software.
2. Analysis of BER, EVM and constellation for Digital modulation techniques.
3. Wave form generation and play back operation using vector signal generator and VSA hardware.
4. Frequency domain measurements using Signal analyser.
5. Time domain measurements using Mixed signal oscilloscope.

REFERENCES:

1. Theodore S Rappaport, "Wireless Communications", Pearson Education, Asia , New Delhi, 2009
2. Gordon L Stuber, "Principles of Mobile Communication", Artech House, 2011.
3. Valeria Teppati, Andrea Ferrero and Mohamed Sayed "Modern RF and Microwave Measurement Techniques", Cambridge University Press, 2013.
4. Ananjan Basu "An Introduction to Microwave Measurements" CRC Press, 2015.
5. Matthew M Radmanesh "RF & Microwave Design Essentials" Author house, 2007.
6. Hsiao-Hwa Chen and Mohsen Guizani, "Next Generation Wireless Systems and Networks, John Wiley & Sons, 2006.

15LV43/15LW47/15LC48 EMBEDDED SYSTEM DESIGN

3 2 0 4

EMBEDDED DESIGN CYCLE: Differences between the Desktop PC and typical Embedded System-Examples of Embedded Systems-Major hardware and software modules of an embedded system-Product Specification, Hardware/Software Partitioning, Iteration and Implementation, Detailed Hardware and Software Design, Hardware Software Integration, Product Testing and Release, Maintenance and Upgrading Existing products. (4)

REVIEW OF EMBEDDED ARCHITECTURES: CPU Core**,** Clock and Reset Generator, PLL, RTC, Program Memory, Data Memory, EEPROM, Parallel Ports, Timers/Counters, Watch-dog timers, input-Capture/Output Compare units, PWM unit, Interrupt Structure, Data converters, Serial communication using SCI, SPI, I2C, CAN and USB - Introduction to LIN and MOST - Development and debugging Support: JTAG and BDM. (12+6)

EMBEDDED SOFTWARE DEVELOPMENT TOOLS: Host and Target Machines, Cross-Compilers, Cross-Assemblers, Linker/Locator for Embedded Software, Locator Maps, Intel hex file format/Motorola s-record format. Introduction to Integrated

Development Environment (IDE)- programming concepts and embedded programming in C. Debugging and simulation techniques, Programming the target system. (8+3)

PERIPHERAL PROGRAMMING: Developing device drivers, Configuring and programming of ports, timer / counter, data converters, interrupts and serial communication. (6+6)

REAL TIME OPERATING SYSTEMS (RTOS): Survey of software architectures, hard/soft real time systems, Tasks and Task States, Tasks and Data, Semaphores and Shared Data, Message Queues, Mailboxes and Pipes, Timer functions, Events, Memory Management, Interrupt Routines in RTOS Environment. (8+6)

CASE STUDY: Study and analysis of generating low frequency bio signals, High power signal analysis using Mixed Signal oscilloscopes, FPGA Debugs and host of serial protocols like CAN/LIN,USB, RS232/UART, I²C/SPI, MIL-STD 1553/ARINC 429, I²S, Application development in ARM micro controllers / Micro controllers / DSP controllers, Programming with RTOS. (7+9)

Total L: 45 + T: 30 = 75

TUTORIAL COMPONENT:

1. Parallel Port programming and interfacing of I/O devices.
2. Interrupt programming: Timer interfacing and analyzing capture compare module.
3. Serial port interfacing.
4. Serial protocol analyzing: RS232 / RS485 / SPI / SCI / I2C / CAN / USB.
5. Programming and Interfacing of data converters.

REFERENCES:

1. Rajkamal, “Embedded Systems: Architecture, Programming and Design”, Tata McGraw-Hill, 2006.
2. David E Simon, “An Embedded Software Primer” Pearson Education Asia, 2006.
3. Arnold Berger, “Embedded System Design: An Introduction to Processes, Tools, and Techniques” CMP Books, 2001.
4. Wayne Wolf, “Computers as Components: Principles of Embedded Computing System Design”, Morgan Kuafmann Publishers, 2005.

ONE CREDIT COURSES

For the detailed Syllabi of all the one credit courses offered by Electronics and Communication Engineering department which are listed in this programme scheme refer to the syllabi of M.E Communication Systems programme.

For the detailed syllabi of the electives and one credit courses offered by other departments refer to the syllabi of M.E- Automotive Engineering offered by Automobile Engineering Department.